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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,509	04/20/2001	Paul F. Struhsaker	WEST14-00018	2895

7590  
DOCKET CLERK  
P.O. DRAWER 800889  
DALLAS, TX 75380

EXAMINER
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MOORE, IAN N

ART UNIT	PAPER NUMBER
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2416

MAIL DATE	DELIVERY MODE
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12/16/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 09/839,509	<b>Applicant(s)</b> STRUHSAKER ET AL.	
	<b>Examiner</b> IAN N. MOORE	<b>Art Unit</b> 2416	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 March 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***After Decision by the Board of Patent Appeal and Interference***

1. The Board of Patent Appeals and Interferences reversed all rejections against claim(s) 1-20.

In view of the decision on 9/2/2008, PROSECUTION IS HEREBY REOPENED. The new grounds of rejections are set forth below.

### ***Response to Arguments***

2. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

### ***Specification***

3. The disclosure is objected to because of the following informalities:  
the status of the following reference U.S. application recited in page 1 and 2 must be updated as “**pending**”, “**now issued as U.S. Patent Number**”, or “**now abandoned**”.

- 1) 09/713,684
- 2) 09/838,810
- 3) 09/839,726
- 4) 09/839,719
- 5) 09/839,910
- 6) 09/839,514
- 7) 09/839,512
- 8) 09/839,259

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9) 09/839,457

10) 09/839,075

11) 09/839,499

12) 09/839,458

13) 09/839,456

14) 09/838,924

15) 09/839,727

16) 09/839,734

17) 09/839,513

Appropriate correction is required.

***Claim Rejections - 35 USC § 112 – First Paragraph***

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

**Claim 1** recites, “a high tier that comprises **one or more serial link** is capable of aggregate traffic rates of **up to approximately twenty gigabits per second.**” in lines 4-7.

The broad claim covers two main embodiments:

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**(1) one serial link that is capable of aggregate traffic rate up to approximately twenty gigabits per second.**

(2) more (than one) serial link that is capable of aggregate traffic rate up to approximately twenty gigabits per second.

The specification fails to provide enabling support in such as way to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention claimed **embodiments (1) and (2)** set forth above.

The specification page 32, lines 20 to page 33, lines 2 and lines 13-22 discloses as follows:

**The high tier of backplane 210 comprises** high tier bus 415 and switch matrix cards, 260 and 270. High tier bus 415 supports aggregate traffic rates of up to approximately twenty gigabits per second (20 Gbps). High tier bus 415 uses redundant **high speed serial links** in conjunction with dedicated switch matrix cards, 260 and 270.

**The high speed serial links** are differential low voltage positive emitter coupled logic (LVPECL) levels that are driven from source to destination and are terminated on the receiving end of links. The links are referenced to the 65.536 MHz clock reference that is provided by primary and secondary master timing interface control processor (ICP) cards. This clock rate is **multiplied by twenty (20) by the high speed serial link serial/de-serial devices (SERDES devices) to provide a baud rate of 1.31072 MHz. Because each link is 8B/10B encoded, the corresponding transmission rate is approximately 1.05 Gbps.** In another advantageous embodiment of the present invention, the transmission rate is approximately 2.5 Gbps.

[Emphasis added]

In view of the speciation above, the transmission rate of **one serial link** is only **1.05 Gbps** (giga bit per second) (i.e. approximately 1 Gbps) not “20” Gbps as recited in the claim. Likewise, **two serial link** is only **2.15 Gbps** (giga bit per second) (i.e. approximately 2 Gbps) not “20” Gbps as recited in the claim. Similar scenario applies from three serial links up to nineteen (19) serial links, where 19 serial links traffic rate is **9.45 Mbps**, not “20” Gbps as recited in the claim. One skill in the art would clearly see that 1.05 Gbps or 9.45 Mbps is not the same 20 Gbps

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as recited in the claim. Thus, the applicant disclosure fails to provide enabling disclosure for the claimed invention.

**Claims 10 and 20** are also rejected for the same reason as set forth above in claim 1 since they also disclose the same limitation.

**Claims 2-9 and 11-19** are also rejected since they are depended upon rejected claims as set forth above.

***Claim Rejections - 35 USC § 112 Second Paragraph***

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

**Claim 1** recites, “a high tier that comprises **one or more serial link** is capable of aggregate traffic rates of **up to approximately twenty gigabits per second.**” in lines 4-7.

It is unclear whether “one serial link” has traffic rate twenty gigabits per second or “more than one serial link” have traffic rate twenty gigabits per second. If one serial links already has the “aggregated traffic” traffic rate twenty gigabit per second, then it is impossible for multiple serial link to have the same traffic rate twenty gigabit per second.

**Claims 10 and 20** are also rejected for the same reason as set forth above in claim 1 since they also disclose the same limitation.

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**Claims 2-9 and 11-19** are also rejected since they are depended upon rejected claims as set forth above.

### ***Claim Objections***

8. Claims 1-20 are objected to because of the following informalities:

**Claim 1** recites the clause with the optional language “**capable of**” in lines 3 and 5. In order to present the claim in a better form and to describe a positive or require steps/function to be performing (i.e. using the claim language that does not suggest or make optionally but required steps to be performed), applicant is suggested to revise the claim language such that the steps/functions, which follows “capable of”, to be performed are required (not optional).

**Claims 10, 12 and 20** are also objected for the same reason as set forth above in claim 1.

**Claims 2-9, 11, 13-19** are also objected since they are depended upon objected claims as set forth above.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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10. Claims 10-12 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang (US 20020097713A1).

*(Note that cited Chang disclosure is fully supported by its parent application 60/249871, herein after refers to as Chan'871).*

**Regarding Claim 10**, Chang discloses for use in association with devices such as processors and modems (see page 5, paragraph 14; for using with packet processors and switches that modulates/transforms/switch) used in wireless and wireline access systems (see page 1, paragraph 5-6, in data communication network; note that both wireless and wireline are data communication network systems), a backplane (see FIG. 1, a backplane switch fabric 100; see page 5, paragraph 103, 109; see *Chan'871* sections 2, 3, 6) comprising:

a high tier (see FIG. 2, a combination of “two” (2) links 204; also see *Chan'871* section 2, both FIG.) that comprises one or more serial links (see FIG. 2, that comprises two (2) serial links 204; see page 5, paragraph 106) capable of aggregate traffic rates of up to approximately twenty gigabits per second (see FIG. 2, one serial link 204 provides 10 Giga bit per second (Gb/s) and the aggregate/sum of two (2) serial links 204 provide twenty (20) Gb/s; see page 5, paragraph 105; see page 6, paragraph 111; also see FIG. 3A, a combination of two serial links (i.e. 308A and 308B) provide 10 Gb/s; see page 6, paragraph 120; also see *Chan'871* section 2-5, both FIG.).

**Regarding Claim 11**, Chang discloses a higher tier bus (see FIG. 2, a serial link 204; see page 5, paragraph 103, 109-110; also see *Chan'871* section 2, both FIG.); and

at least two switch matrix circuit boards coupled to said high tier bus (see FIG. 2, Blade matrix/switch circuit board/units 104A, 104B and cross connect switch circuit board/units 202A,

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202B, are connected to a serial link 204; see page 5, paragraph 103, 109-110; see page 6, paragraph 112-113,118; *also see Chan'871 section 2, both FIG.*).

**Regarding Claim 12**, Chang discloses high speed serial links (see FIG. 2, high speed 10Gb/s serial links 204; *also see Chan'871 section 2, both FIG.*) coupled to said at least two switch matrix circuit board cards (see FIG. 2, connects to Blade matrix/switch circuit board/units 104A, 104B and cross connect switch circuit board/units 202A, 202B) and coupled to any other circuit board cards capable of sending and receiving high speed data traffic (see FIG. 2, connect to other Blade matrix/switch circuit board/units 104C, 104D and cross connect switch circuit board/units 202C, 202D,202E; see page 6, paragraph 112-113,118; *also see Chan'871 section 2-5, both FIG.*).

**Regarding Claim 17**, Chang discloses at least two (2) high speed serial links (see FIG. 2, at least two (2) high speed serial links 204; *also see Chan'871 section 2, both FIG.*.) for each interface control processor slot in said back plane (see FIG. 2, for each Blade/interface control/processor slots/units 104 in the backplane; see page 5, paragraph 103, 109-110; see page 6, paragraph 112-113,118; *also see Chan'871 section 2-5, both FIG.*).

### ***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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12. Claims 1-4 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tabu (US 6,560,219) in view of Chang (US 20020097713A1).

*(Note that cited Chang disclosure is fully supported by its parent application 60/249871, herein after refers to as Chan'871).*

**Regarding Claim 1**, Tabu discloses for use in association with devices such as processors and modems (see FIG. 7, using with large and medium processing units) used in wireless and wireline access systems (see col. 6, line 26-35; see col. 7, line 6-10; ATM and STM network system), a bus/switch (see FIG. 7, a bus/switch exchange system; see col. 9, line 41-50) comprising:

a low tier (see FIG. 7, medium unit 2000) that comprises a cell-based bus (see FIG. 7, cell switch/bus/connection 2100 that connects with interface unit 2200 and 2300) capable of aggregate traffic rates of up to approximately two gigabits per second (see col. 9, lines 42-52, 65 to col. 10, line 7-67; capable of switching data rate of 2 Gbps)); and

a high tier (see FIG. 7, large unit 1000) that comprises one or more links (see FIG. 7, comprising one or more link(s)/buse(s) that connects with interface units 1200) capable of aggregate traffic rates of up to approximately twenty gigabits per second (see col. 9, lines 43-54; capable of switching data rate of 20 Gbps).

Although Tabu discloses a bus/switch/connection and one or more links as set forth above,

Tabu does not explicitly disclose “backplane” and “serial”.

However, having it is well known in the art that the backplane is a collection of links/buses that perform switching. In particular, Chang discloses for use in association with

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devices such as processors and modems (see page 5, paragraph 14; for using with packet processors and switches that modulates/transforms/switch) used in wireless and wireline access systems (see page 1, paragraph 5-6, in data communication network; note that both wireless and wireline are data communication network systems), a backplane (see FIG. 1, a backplane switch fabric 100; see page 5, paragraph 103, 109; *also see Chan '871 section 2-5, both FIGs.*) comprising:

a high tier (see FIG. 2, a combination of “two” (2) links 204; *also see Chan '871 section 2-5, both FIGs*) that comprises one or more serial links (see FIG. 2, that comprises two (2) serial links 204; see page 5, paragraph 106) capable of aggregate traffic rates of up to approximately twenty gigabits per second (see FIG. 2, one serial link 204 provides 10 Giga bit per second (Gb/s) and the aggregate/sum of two (2) serial links 204 provide twenty (20) Gb/s; see page 5, paragraph 105; see page 6, paragraph 111; *also see FIG. 3A, a combination of two serial links (i.e. 308A and 308B) provide 10 Gb/s; see page 6, paragraph 120; also see Chan '871 section 2-5, both FIGs*).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide “backplane” and “serial” as taught by Chang in the system of Tabu, so that it would provide a high performance switch backplane that use the serial link technology that is capable of a high performance a maximum aggregate bit carrying capability; see Chang page 1, paragraph 11-12.

**Regarding Claim 2**, Tabu discloses a low tier bus comprising a switching architecture (see FIG. 7, cell switch/bus 2100 performs switching) that

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(1) allows a circuit board card (see FIG. 7, interface unit 2200) on an input side of a connection (see FIG. 7, on the input side of a connection) to transmit data to a circuit board card on an output side of said connection (see FIG. 7, to transmit cell data to interface unit 2300 on the output side of the connection; see col. 9, lines 42-52, 65 to col. 10, line 67), and that

(2) allows a circuit board card (see FIG. 7, interface unit 2300) on an output side of a connection (see FIG. 7, on the output side of a connection) to receive data from a circuit board on the input side of said connection (see FIG. 7, to receive cell data to interface unit 2200 on the input side of the connection; see col. 9, lines 42-52, 65 to col. 10, line 7-67)).

**Regarding Claim 3**, Tabu discloses wherein said low tier bus supports one of packet based traffic (see FIG. 7, cell switch/bus/connection 2100 switch ATM cell/packet base data/traffic; see col. 9, lines 65 to col. 10, line 7).

**Regarding Claim 4**, Tabu discloses wherein said low tier bus supports asynchronous transfer mode traffic (see FIG. 7, cell switch/bus/connection 2100 switch ATM cell/packet base data/traffic; see col. 10, lines 1-9).

**Regarding Claim 20**, Tabu discloses a device comprising a bus/switch see FIG. 7, a bus/switch exchange system; see col. 9, line 41-50):

a low tier (see FIG. 7, medium unit 2000) that comprises a cell-based bus (see FIG. 7, cell switch/bus/connection 2100 that connects with interface unit 2200 and 2300) capable of aggregate traffic rates of up to approximately two gigabits per second (see col. 9, lines 42-52, 65 to col. 10, line 7-67; capable of switching data rate of 2 Gbps)); and

a high tier (see FIG. 7, large unit 1000) that comprises one or more links (see FIG. 7, comprising one or more link(s)/buse(s) that connects with interface units 1200) capable of

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aggregate traffic rates of up to approximately twenty gigabits per second (see col. 9, lines 43-54; capable of switching data rate of 20 Gbps);

wherein said device comprises one of: an access processor unit (see FIG. 7, a control unit (CC) that performs processing; see col. 7, line 10-15).

Although Tabu discloses a bus/switch/connection and one or more links as set forth above,

Tabu does not explicitly disclose “backplane” and “serial”.

However, having it is well known in the art that the backplane is a collection of links/buses that perform switching. In particular, Chang discloses a device comprising a backplane (see FIG. 1-2, a high performance network switch comprising a backplane switch fabric 100 (see FIG. 2); see page 5, paragraph 103, 109; *also see Chan '871 section 2-5, both FIGs*) comprising:

a high tier (see FIG. 2, a combination of “two” (2) links 204; *also see Chan '871 section 2-5, both FIGs*) that comprises one or more serial links (see FIG. 2, that comprises two (2) serial links 204; see page 5, paragraph 106) capable of aggregate traffic rates of up to approximately twenty gigabits per second (see FIG. 2, one serial link 204 provides 10 Giga bit per second (Gb/s) and the aggregate/sum of two (2) serial links 204 provide twenty (20) Gb/s; see page 5, paragraph 105; see page 6, paragraph 111; also see FIG. 3A, a combination of two serial links (i.e. 308A and 308B) provide 10 Gb/s; see page 6, paragraph 120; *also see Chan '871 section 2-5, both FIGs*);

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wherein said device comprises one of: an access processor unit (see FIG. 3A, super backplane interface adaptor (SBIA) for processing the data the backplane; see page 6, paragraph 119; *also see Chan'871 section 2-5, both FIGs*).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide “backplane” and “serial” as taught by Chang in the system of Tabu, so that it would provide a high performance switch backplane that use the serial link technology that is capable of a high performance a maximum aggregate bit carrying capability; see Chang page 1, paragraph 11-12.

13. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tabu in view of Chang as applied to claims above, and further in view of Chui (U.S. 6,512,769).

**Regarding Claim 5**, Tabu discloses transmitting of asynchronous transfer mode cells as set forth above in claim. Tabu further discloses allow said lower tier bus to switch cell based traffic to each circuit board connected to said lower tier bus (see FIG. 7, cell switch/bus/connection 2100 switches ATM cells to each interface unit 2200/2300 connected to , cell switch/bus/connection 2100; see col. 9, lines 42-52, 65 to col. 10, line 67).

Neither Manchester nor Tabu explicitly discloses “wraps asynchronous transfer mode cells with a header” and “according to the connection map”.

However, Chui discloses a lower tier bus (see FIG. 6, cell BUS) wraps asynchronous transfer mode cells with a header (see FIG. 9, ATM cell is encapsulated with cell bus header byte; see col. 8, lines 1-6) to allow to said lower tier bus to switch cell based traffic according to the connection map (see FIG. 24-25, connection address map RAM data) on each circuit board

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card (see FIG. 6; cards 606-608,610-612) connected to said low tier bus (see col. 5, lines 60 to col. 6, lines 67; see col. 14, lines 30-65).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide “wraps asynchronous transfer mode cells with a header” and “according to the connection map”, as taught by Chui, in the combined system of Tabu and Chang, so that it would provide fair rate-based cell traffic arbitration and provide flexibility and a performance improvement in the translation of cell routing information; see Chui col. 2, lines 40-65.

14. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tabu and Chang as applied to claims above, and further in view of Ahmadi (US 5,008,878).

**Regarding Claim 6**, the combined system of Tabu and Chang discloses said lower tier bus as set forth in claims above.

Neither Tabu nor Chang explicitly discloses “two (2) parallel buses, each of which comprises a thirty two (32) bit data path”.

However, a data bus having 32 bit data path is well known in the art. In particular, Ahmadi discloses a low tier bus (see FIG. 12, 13, bus 103) comprising two (2) parallel buses (see FIG. 13, two parallel buses of even bus 103b and odd bus 103a), each of which comprises a thirty two (32) bit data path (see FIG. 13, each bus has 32 bits data path/lines; see abstract, col. 2, lines 5-15; see col. 11, lines 45-62).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide “two (2) parallel buses, each of which comprises a thirty two

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(32) bit data path”, as taught by Ahmadi, in the combined system of Tabu and Chang, so that it would provide fast switching apparatus which accommodate very high speed traffic in a unified manner; see Ahmadi col. 2, line 31-36.

15. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tabu and Chang as applied to claims above, and further in view of Donati (US 7,007,099).

**Regarding Claim 7**, the combined system of Tabu and Chang discloses said lower tier bus in said back plane as set forth in claims above.

Neither Tabu nor Chang explicitly discloses “a clock rate equal to one half of a clock rate”.

However, Donati discloses wherein said low tier bus operates at a clock rate (see FIG. 29A, a link/bus clock rate is 32.768 MHz) equal to one half of a clock rate of said backplane/bus (see FIG. 29A, which is a half of a system/bus clock rate 65.536 MHz; see col. 41, line 5-15).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide “a clock rate equal to one half of a clock rate”, as taught by Donati, in the combined system of Tabu and Chang, so that it would provide improve serial to bus interface to allow rapid data exchange; see Donati col. 1, line 45-67.

**Regarding Claim 8**, the combined system of Tabu and Chang discloses said lower tier bus in said back plane as set forth in claims above.

Neither Tabu nor Chang explicitly discloses “32.768 MHz”.

However, Donati discloses wherein said low tier bus clock rate is 32.768 MHz (see FIG. 29A, a link/bus clock rate is 32.768 MHz; see col. 41, line 5-15).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide “32.768 MHz”, as taught by Donati, in the combined system of Tabu and Chang, so that it would provide improve serial to bus interface to allow rapid data exchange; see Donati col. 1, line 45-67.

16. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tabu and Chang, as applied to claims above, and further in view of Pajowski (U.S. 5,355,090).

**Regarding Claim 9**, the combined system of Tabu and Chang discloses said lower tier bus and a clock reference as set forth in claims above.

Neither Tabu nor Chang explicitly discloses “a redundant clock reference”.

However, having a redundant clock reference is well known in the art. Pajowski discloses a redundant clock reference for a low tier system (see FIG. 1, see abstract; col. 2, lines 44-65; redundant clock system for bus system).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide “a redundant clock system”, as taught by Pajowski, in the combined system of Tabu and Chang, so that it would over timing problems by reducing timing errors; see Pajowski col. 2, line 5-40.

17. Claim 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tabu and Chang, as applied to claims above, and further in view of Panzarella (U.S. 5,416,776).

**Regarding Claim 18**, the combined system of Tabu and Chang discloses the backplane as set forth in claim above.

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Neither Tabu nor Chang explicitly disclose “one of a time division multiplex bus, a common control bus”.

However, implementing a common/control bus in the backplane is well known in the art. In particular, Panzarella discloses one of a time division multiplex bus (see FIG. 1, TDM bus 201) and a common control bus (see FIG. 1, Management bus 401; see col. 3, lines 60 to col. 4, lines 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide one of a time division multiplex bus, a common control bus”, as taught by Panzarella, in the combined system of Tabu and Chang, so that it would provide a backplane which capable of enabling high speed network communication among larger number of modems and related circuits and increasing the number of buses which offers distinct advantages for chassis requiring a substantial number of modems and related circuit boards; see Panzarella col. 1, line 20 to col. 2, lines 4.

**Regarding Claim 19**, Tabu discloses at least one set of framing resources (see FIG. 7, a bus/switch exchange system comprising switching/framing units/resources that frame and switch ATM and STM data; see col. 9, line 41-50).

Tabu does not explicitly disclose “backplane” and at least “one set of clock”.

However, Chang discloses a backplane (see FIG. 1, a backplane switch fabric 100; see page 5, paragraph 103, 109; *also see Chan ’871 section 2-5, both FIGs*) comprising at least one set of clock (see page 14, paragraph 215, 223,227; clock 1714 (see FIG. 17), or referee clock 1828/1820 (see FIG. 18)) and framing resources (see page 5, paragraph 103,109; see page 6, paragraph 118, 119; see page 7, paragraph 128-129; packet processor/encoder (i.e. packet

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processing resources) packetized/encode/frame the packets; see FIG. 18-20; *also see Chan '871 sections 2-9*).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide “backplane” and at least “one set of clock” as taught by Chang in the system of Tabu, so that it would provide a high performance switch backplane that use the serial link technology that is capable of a high performance a maximum aggregate bit carrying capability; see Chang page 1, paragraph 11-12.

Also, Panzarella discloses at least one set of clock and framing resources (see col. 3, lines 5-14, 45-67 and see col. 4, lines 14-30; clocking and framing/packaging resources).

18. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang in view of Lewis (U.S. 6,754,757).

**Regarding Claim 13**, Chang discloses point-to-point serial links (see FIG. 2, serial links 204) comprising pairs for both a transmit path and receive path (see col. 2, two directional arrows of serial link 204 (i.e.  $\Leftrightarrow$ ) indicates that there is a pair of transmit and receive paths; see page 5, paragraph 103, 109-110; see page 6, paragraph 112-113, 118).

Chang does not explicitly disclose “differential” pair.

However, Lewis teaches point-to-point serial links comprising differential pairs for both a transmit path and receive path (see FIG. 2, point to point serial links with differential pair, Tx pair and Rx pair, for transmit and receive paths/links; see col. 2, line 20-25, 60 to col. 3, line 5; see col. 4, line 40-45).

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Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide differential” pair as taught by Lewis in the system of Chang, so that it would improve the speed of the communication going over a backplane ; see Lewis col. 1, line 20-45.

19. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang and Lewis, as applied to claims above, and further in view of Chesavage (U.S. 6,239,626).

**Regarding Claim 14**, Chang discloses said high speed serial links operates at a clock rate (see page 6, paragraph 12; link clock with 133 MHz operating at 4 Gb/s rate) and backplane clock rate (see page 6, paragraph 122-123,150; backplane clock 156.25MHz operation at the clock rate 4 times the data rate; also see paragraphs 190, 205, 210, 215, 219, 223, 227, 234, 240; *also see Chan’871 section 2-9*).

Although Chang discloses said high speed serial links clock rate and backplane clock rate as set forth above,

neither Chang nor Lewis explicitly discloses operating at a clock rate “equal to”.

However, Chesavage discloses said links operates at a clock rate equal to a clock rate of said backplane (see FIG. 7, each links connects to line cards 4-7 operates at a clock rate equal to the backplane 141 SYSCLK clock rate produced by a clock generator 170 (see FIG. 8); see col. 5, line 32-65).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide operating at a clock rate “equal to”, as taught by Chesavage, in the combined system of Chang and Lewis, so that it would provide a glitch-free clock

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selection between two frequency and phase locked sources without producing output transients; see Chesavage col. 2,, line 10-22.

20. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang and Lewis and Chesavage, as applied to claims above, and further in view of Petty (U.S. 5,862,131).

**Regarding Claim 15**, the combined system of Chang, Lewis and Chesavage discloses said high speed serial links clock rate as set forth in claims above.

Neither Chang, Lewis nor Chesavage explicitly disclose “65.536 MHz”.

However, Petty discloses said link clock rate is 65.536 MHz (see FIG. 2, port where the link is connected has a clock line 215 is 65.536 MHz; see col. 4, line 20-25).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide “65.536 MHz”, as taught by Petty, in the combined system of Chang, Lewis and Chesavage, so that it would increase the bus capacity that is easily retrofitted into existing system and does not interfere with the operation; see Petty col. 1, line 35-56.

21. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang and Lewis and Chesavage, as applied to claims above, and further in view of Momtaz (U.S. 5,950,115).

**Regarding Claim 15**, Chang discloses said high speed serial/de-serial device that communicates with said high speed serial link (see FIG. 5, serializer 580/deserializer 510 communicates with high speed links from the ports 401; see page 7-18, paragraph 129,133,136,142,150,232-235, 240, 243, 247, 250, 252, 272, 294; also see FIG. 8-9) and wherein each high speed serial links is encoded (see FIG. 18, encoders 1814; see FIG. 19, encoders 1912,

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1918; high speed serial links is encoded; see paragraphs 97, 112, 135, 144, 152, 159, 162, 164 165, 170 ,171, 177, 181, 195, 204, 211, 214, 215, 240, 247, 252, 284; *also see Chan'871 section 2-9*).

Neither Chang, Lewis nor Chesavage explicitly disclose “multiplies by a factor” and “8B/10B” encoded.

However, Momtaz discloses a link device that multiplies said link clock rate by a factor of ten (10) (see col. 7, line 40-60; see col. 8, line 5-15, 35-45; see col. 11, line 30-52; VCO 76 is locked at multiple of ten time the speed of link clock reference), and wherein each high speed serial link is 8B/10B encoded (see col. 7, line 1-18; high speed link is coded at 8B/10B; see col. 4, line 20-25).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide “multiplies by a factor” and “8B/10B” encoded”, as taught by Momtaz, in the combined system of Chang, Lewis and Chesavage, so that it would adapt to interface between high-speed serial data and encoded transmission; see Momtaz col. 4, line 67 to col. 5, line 5.

Although Momtaz discloses a link device that multiplies said link clock rate by a factor of ten (10) (see col. 7, line 40-60; see col. 8, line 5-15, 35-45; see col. 11, line 30-52; VCO 76 is locked at multiple of ten time the speed of link clock reference),

neither Chang, Lewis, Chesavage nor Momtaz explicitly disclose multiplies of “twenty (20)”.

However, multiplying the clock rate by 20 does not define a patentable distinct invention over that in the combined system because Momtaz discloses the multiplication by integer value

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preferably “10”, since the invention as a whole and the combined system is directed to meet the functional needs of the switch. The degree in which multiplying clock rate by twenty (20) instead of ten (10) presents no new or unexpected results (i.e. the higher the clock rate, the higher the speed, and the lower the clock rate, the lower the speed), as long as the switch performs and meet its functional needs. Therefore, to multiply the clock rate by twenty would have been routine experimentation and optimization in the absence of criticality.

### ***Conclusion***

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to IAN N. MOORE whose telephone number is (571)272-3085.

The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Trost can be reached on 571-272-7872. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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